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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,309	10/03/2003	Tetsuo Suzuki	243579US0X	9488

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OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
GRAMAGLIA, MAUREEN	

ART UNIT	PAPER NUMBER
1792	

NOTIFICATION DATE	DELIVERY MODE
04/24/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@oblon.com
oblonpat@oblon.com
jgardner@oblon.com

Office Action Summary	Application No.	Applicant(s)	
	10/677,309	SUZUKI ET AL.	
	Examiner	Art Unit	
	Maureen Gramaglia	1792	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2009 and 21 February 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5-24 and 27-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-24 and 27-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submissions filed on 21 January 2009 and 21 February 2009 have been entered.

Claim Objections

2. Claims 8, 9, 11, and 12 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Specifically, Claims 8, 9, 11, and 12 recite claim limitations now recited in independent Claim 1 as amended.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 14-24, 28, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 3,923,567 to Lawrence in view of U.S. Patent

6,100,167 to Falster et al. and U.S. Patent 5,622,875 to Lawrence (herein referred to as US '875).

In regards to Claim 1, Lawrence teaches a method of reclaiming silicon wafers that includes, in the following order, a film removal process (Column 5, Lines 52-65), a heating/removal process (Column 6, Lines 6-33 and Line 49 - Column 7, Line 31), a polishing process (Column 7, Lines 32-38), and a cleaning process (Column 7, Lines 38-40), wherein the heating / removal process is between the film removal process and the polishing process and comprises heating the silicon wafer (Column 6, Lines 6-33) and a chemical process carried out "in air" in that the chemical processing tank would be surrounded by air, that comprises removing a surface part of the silicon wafer by etching the top surface of the silicon wafer (Column 6, Line 49 - Column 7, Line 24).

In regards to Claim 1, Lawrence does not expressly teach that the heating of the silicon wafer is performed at 150-300°C for 20 minutes - 5 hours. In regards to Claim 15, Lawrence does not expressly teach that the heating step of the heating/removal process is carried out in air. In regards to Claim 16, Lawrence does not expressly teach that the maximum temperature is 300°C.

Falster et al. teaches in a method of reclaiming silicon wafers (Column 1, Lines 11-13) a heating / removal process comprising heating the silicon wafer at 100-300°C for a preferred time of several to several tens of minutes up to about 1.5 hours. (Column 3, Line 61 - Column 4, Line 10) These ranges in temperature and time meet the limitations recited in Claim 1. Falster et al. further teaches that heating process can

be carried out in air (Column 4, Lines 16-18), and that the maximum temperature can be 300°C (Column 4, Line 3).

(The Examiner also observes that Falster et al. (Column 3, Lines 51-60) further teaches that the time is a result-effective variable that affects the diffusion of copper to the surface of the silicon wafer, and is selected in accordance with the heating temperature.)

It would have been obvious to one of ordinary skill in the art to replace the heating step of the heating / removal process taught by Lawrence with the heating step taught by Falster et al. The motivation for making such a modification, as taught by Falster et al. (Column 2, Line 67 - Column 3, Line 50), would have been to diffuse copper to the surface of the silicon wafer without the undesirable copper precipitates that form when the heating is performed at higher temperatures. Moreover, Falster et al. expressly teaches that the heating step taught by Falster et al. is an improvement over prior art gettering methods, since the high diffusivity of copper in silicon makes it possible for copper to escape from the gettering sites and reach the device region of the wafer. (Column 1, Line 64 - Column 2, Line 3)

Further in regards to Claims 1 and 23, the combination of Lawrence and Falster et al. does not expressly teach that the chemical removal step comprises etching the silicon wafer with a solution comprising an alkaline (i.e. basic) hydroxide to a depth of 1 micron.

US '875 teaches, in a method of reclaiming a silicon wafer (Column 4, Lines 31-42), a chemical removal step comprising etching the silicon wafer with a solution comprising KOH to a depth of at least 1 micron. (Column 8, Lines 13-31)

It would have been obvious to one of ordinary skill in the art to further modify the method taught by the combination of Lawrence and Falster et al. to have the chemical removal solution comprise KOH, as an art-recognized suitable etchant as taught by US '875 for that purpose, and to etch the silicon wafer to a depth of at least 1 micron, in order to, as taught by US '875 (Column 8, Lines 13-31), remove impurities from the wafer and to remove an unwanted top surface layer of silicon having considerable crystalline strain.

In regards to Claim 30, the heating/removal process of the combination of Lawrence, Falster et al., and US '875 can be defined such that the only chemical process is the chemical etching step, i.e. immersing the silicon wafer in the solution comprising KOH.

In regards to Claim 2, Lawrence teaches that the heating / removal process can further include a mechanical removal process (Column 7, Lines 25-31).

In regards to Claims 14, 17, and 18, the heating step of the heating/removal process taught by the combination of Lawrence and Falster et al. is carried out so as to provide a *P-type silicon wafer* having the same specific resistance of a virgin (i.e. unused) P-type silicon wafer, as broadly recited in the claims. (Falster et al., Column 1, Line 11 - Column 2, Line 50; Column 3, Line 12 - Column 4, Line 18; Column 5, Lines 14-29) The heating step of the heating/removal process as taught by the *combination*

of Lawrence and Falster et al. would inherently not form any oxygen donors, since the process is performed below 300°C and no dopant is introduced into the wafer. This rejection is based on the fact that the method taught by the *combination* of Lawrence and Falster at al. would inherently result in the reclaimed wafer having the recited properties. When a rejection is based on inherency, a rejection under 35 U.S.C. 102 or U.S.C. 103 is appropriate. (See *In re Fitzgerald* 205 USPQ 594 or MPEP 2112).

In regards to Claims 19, 20, and 22, Lawrence teaches that the method can be carried out to reclaim silicon wafers that were previously used as testing wafers to carry out the monitoring of a semiconductor chip manufacturing process. (*The wafers can be classified as process monitor test wafers…*; Column 1, Lines 30-40; Column 5, Lines 32-35)

In regards to Claim 21, the wafer reclamation method taught by the combination of Lawrence, Falster, and US '875 would inherently produce a silicon wafer without Cu contamination, as broadly recited in the claim (i.e. produce a silicon wafer with a level of contaminants at or below that of a virgin wafer), since the process taught by the combination of Lawrence and Falster et al. is carried out so as to remove contaminants and provide a *P-type silicon wafer* having the same specific resistance of a virgin (i.e. unused) P-type silicon wafer, as discussed above, and the alkaline chemical etching step taught by the combination of Lawrence, Falster et al., and US '875 etches the wafer to a depth of 1 micron. This rejection is based on the fact that the method taught by the *combination* of Lawrence, Falster at al., and US '875 would inherently result in the reclaimed wafer having the recited properties. When a rejection is based on

inherency, a rejection under 35 U.S.C. 102 or U.S.C. 103 is appropriate. (See *In re Fitzgerald* 205 USPQ 594 or MPEP 2112).

5. Claims 5-13 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lawrence in view of Falster et al. and US '875 as applied to claim 1 above, and further in view of U.S. Patent 5,932,022 to Linn et al.

The teachings of Lawrence, Falster et al., and US '875 were discussed above.

In regards to Claims 5, 6, and 29, the combination of Lawrence, Falster et al., and US '875 does not expressly teach that an immersion process for chemically processing the silicon wafer (which would contact the top surface of the silicon wafer) with at least one of an SC-1 or SC2 liquid should be performed in addition to the heating / removal process between the film removal process and the polishing process, or that the processing liquid can be any of the liquids recited in Claim 6.

Linn et al. teaches an immersion process for chemically processing a bare silicon wafer should be performed prior to a heating step 115 (Figure 1), wherein the processing liquid can be a mixed solution of hydrogen peroxide, ammonia, and water (SC-1 cleaning solution; Step 101; Column 3, Lines 13-20), or a mixed solution of hydrogen peroxide, hydrochloric acid, and water (SC-2 cleaning solution; Step 109; Column 3, Lines 55-65).

It would have been obvious to one of ordinary skill in the art to modify the combination of Lawrence, Falster et al., and US '875 to include an immersion process for chemically processing the wafer with an SC-1 or SC-2 liquid just before the heating / removal step, with processing liquids taught by Linn et al. The motivation for making

such a modification, as taught by Linn et al. (Column 4, Lines 43-49), would have been to perform the heating step on a wafer with a relatively metal-free, hydrophilic surface, such that the finally processed wafer has an increased minority carrier diffusion length.

In regards to Claims 7, 8, 10, and 11, Lawrence teaches that the heating / removal process can include a mechanical removal process (Column 7, Lines 25-31) and a chemical removal process (Column 6, Line 49 - Column 7, Line 21).

In regards to Claims 9, 12, and 13, the combination of Lawrence, Falster et al., and US '875 as applied to Claim 1 above teaches that the chemical removal step can be performed using alkaline hydroxides, specifically potassium hydroxide.

6. **Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lawrence in view of Falster et al. and US '875 as applied to claim 1 above, and further in view of U.S. Patent Application Publication 2004/0108297 to Erk et al.**

The teachings of Lawrence, Falster et al., and US '875 were discussed above.

In regards to Claim 24, the combination of Lawrence, Falster et al., and US '875 does not expressly teach that the wafer is etched in the chemical removal step with a solution comprising an alkaline carbonate.

Erk et al. teaches that an etching solution for silicon wafers can comprise an alkaline hydroxide, and additionally an alkaline carbonate, such as potassium carbonate. (Paragraphs 43, 48, and 54-63)

It would have been obvious to one of ordinary skill in the art to modify the etching solution for the chemical removal step taught by the combination of Lawrence, Falster et al., and US '875 to further comprise an alkaline carbonate, such as potassium

carbonate, as taught by Erk et al. The motivation for making such a modification, as taught by Erk et al. (see at least Paragraphs 61-63), would have been that the addition of a salt additive such as potassium carbonate contributes to improved surface characteristics of the etched wafer.

7. **Claims 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lawrence in view of Falster et al. and US '875 as applied to claim 1 above, and further in view of Erk et al. and U.S. Patent 5,810,940 to Fukazawa et al.**

The teachings of Lawrence, Falster et al., and US '875 were discussed above.

In regards to Claim 26, the combination of Lawrence, Falster et al., and US '875 does not expressly teach that the chemical process of the heating/removal process further comprises top surface cleaning the silicon wafer with an aqueous solution comprising hydrofluoric acid and hydrogen peroxide after etching.

Erk et al. teaches that a wafer should be cleaned after etching. (Paragraph 80)

It would have been *prima facie* obvious to one of ordinary skill in the art to include a cleaning step after etching the silicon wafer in the chemical removal process of Lawrence, Falster et al., and US '875, for the predictable result of washing off the spent etchant and other impurities from the surface of the silicon wafer.

Fukazawa et al. teaches that an aqueous solution comprising hydrofluoric acid and hydrogen peroxide is a suitable cleaning solution for a silicon wafer, especially for removing copper impurities from the surface of the wafer. (see at least Column 5, Lines 11-15 and Column 6, Lines 16-20)

It would have been *prima facie* obvious to one of ordinary skill in the art to use an aqueous solution comprising hydrofluoric acid and hydrogen peroxide to clean the silicon wafer after etching in the method taught by the combination of Lawrence, Falster et al., US '875, and Erk et al., as an art-recognized suitable cleaning solution, as taught by Fukazawa et al., for the intended purpose of cleaning and removing copper impurities from the surface of the silicon wafer.

In regards to Claim 27, the Cu concentration of the silicon wafer after said top cleaning step in the combination of Lawrence, Falster et al., US '875, Erk et al., and Fukazawa et al. would inherently be no more than 2×10^{12} atom/cm^3, since the combination of Lawrence, Falster et al., US '875, Erk et al., and Fukazawa et al. teaches an identical chemical processing method to that claimed by Applicant, and the action of the same chemical processing steps to a contaminated silicon wafer would be expected to have the same results as those disclosed by Applicant. When a rejection is based on inherency, a rejection under 35 U.S.C. 102 or U.S.C. 103 is appropriate. (See *In re Fitzgerald* 205 USPQ 594 or MPEP 2112).

Response to Arguments

8. Applicant's arguments filed 21 January 2009 have been fully considered but they are not persuasive.

Applicant argues that Falster is not relevant to reclaiming used silicon wafers, but only removing copper from a polished surface. Applicant further argues that one of ordinary skill in the art would not substitute only the annealing step of Falster for the gettering step of Lawrence '567, but at best would only substitute the annealing/cleaning

of Falster for the gettering/etching of Lawrence '567, and that such a substitution would exclude etching and thus be contridictory to the claimed limitation of etching to a depth of about 1 micron. These arguments are not persuasive. Examiner maintains that Falster is actually concerned with removing copper that has diffused to the interior of the silicon wafer (ex. Column 2 of Falster), and that both Lawrence '567 and Falster are concerned with solving the same problem of removing contaminants from the interior of the wafer. One of ordinary skill in the art, taking the teachings of Lawrence '567 and Falster as a whole, would recognize that the etching step of one versus the cleaning step of the other are not contridictory teachings, but rather directed to the same goal of removing contaminants that have been moved to the surface of the wafer, and differing only in degree. The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Applicant argues that it is non-obvious to employ the teachings of Lawrence '875, since Lawrence '875 teaches only to remove impurities from the edge of a silicon wafer, not the top surface. Examiner mantained that it would still be obvious to employ the teachings of Lawrence '875, since Lawrence '875 teaches a suitable silicon etchant. Again, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the

claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Applicant argues that etching with an alkaline solution provides a means of reducing the Cu concentration in silicon wafers by an amount that is substantially greater than the amount of Cu reduction that is achieved with other types of etching. However, Examiner notes that the combination of Lawrence, Falster, and US '875 applied to Claim 1 teaches etching the silicon wafer using an alkaline solution to a depth of 1 micron, and therefore, by applying the same chemical processing steps as Applicant, would be expected to produce the same result of reduced Cu contamination.

Applicant argues that the data presented in the Specification, specifically in Figure 3, is evidence that performing an alkaline etch plus acidic cleaning gives an unexpected result, by reducing copper contamination below the limit of detection. Examiner maintains that while the data in the specification may indicate that different results are obtained using the inventive method versus Applicant's admitted prior art method, it is not clear that any such differences are unexpected. Examiner indicated that because the chart of Figure 3 compares the results of single step cleaning methods to the result of a two-step etching and cleaning, it is not clear that getting better results with a two-step method versus a single step method would be unexpected. Examiner asserts that one of ordinary skill in the art would expect to get an even cleaner wafer

with a two-step etch and clean, and that a *prima facie* case of obviousness for the claimed method has been clearly set forth above.

Examiner notes Applicant's arguments regarding newly presented claims 29 and 30. A *prima facie* case of obviousness has been established above regarding these claims.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Maureen Gramaglia whose telephone number is (571)272-1219. The examiner can normally be reached on core hours of 10-5, Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Parviz Hassanzadeh can be reached on (571) 272-1435. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Maureen Gramaglia/
Examiner, Art Unit 1792

/Parviz Hassanzadeh/
Supervisory Patent Examiner, Art Unit 1792